

UNITED STATES PATENT APPLICATION
FOR
DUAL GATE NITRIDE PROCESS
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DESCRIPTION OF THE INVENTION

Field of the Invention

[001] The present invention pertains to in general a method for manufacturing a semiconductor device, and, more particularly, to a method for forming a dual gate nitride structure.

Background of the Invention

[002] Modern integrated circuits ("ICs") are designed to perform multiple functions. For example, many ICs include logic circuits as well as memory elements to enable the ICs to perform logic functions and store data. One conventional manufacturing process for such ICs provides multiple gate oxide thicknesses in a single oxide layer. A "dual-gate-oxide-thickness" process is one conventional manufacturing process that forms a single oxide layer with two varying thicknesses. Generally, the dual-gate-oxide-thickness process involves two oxidation steps with a masked etching step between the two oxidation steps to decrease the thickness of certain regions of the oxide layer. However, as the devices continue to be scaled to sub-micron dimensions, the etching process becomes problematic and a strong gate oxide layer becomes increasingly difficult to obtain.

[003] Another conventional approach to providing dual gate oxide thicknesses is through nitrogen implantation because the oxidation rate may be slowed when nitrogen is present in silicon layer upon which the oxidation process takes place. Therefore, selective implantation of nitrogen will allow the formation of thicker oxide portions in non-implanted silicon regions and thinner oxide portions in nitrogen implanted silicon regions. However, nitrogen implantation sometimes

creates implantation-induced defects that would be inevitably incorporated into the oxide layer through the oxidation process. These defects may degrade the gate oxide integrity. In addition, the implanted nitrogen might be unintentionally diffused further into the silicon layer during the high-temperature oxidation process. As a result, oxide thickness and uniformity become difficult to predict or control.

SUMMARY OF THE INVENTION

[004] In accordance with the invention, there is provided a method of manufacturing a semiconductor device that includes providing a wafer substrate having a surface, forming a first nitride layer over the wafer substrate, providing a layer of photoresist over the first nitride layer, patterning and defining the photoresist layer, etching the first nitride layer unmasked by the photoresist to remove at least a portion of the first nitride layer to expose at least a portion of the substrate surface, removing the photoresist layer, and depositing a second nitride layer over the first nitride layer and the exposed substrate surface to form a nitride structure having a first thickness and a second thickness, wherein the first thickness includes a thickness of the first nitride layer.

[005] Also in accordance with the invention, there is provided a method of manufacturing a semiconductor device that includes providing a wafer substrate having a surface, forming a first nitride layer over the wafer substrate, providing a layer of photoresist over the first nitride layer, patterning and defining the photoresist layer, etching the first nitride layer unmasked by the photoresist to remove at least a portion of the first nitride layer to expose at least a portion of the substrate surface, removing the photoresist layer, and depositing a second nitride layer over the first

nitride layer and the exposed substrate surface to form a nitride structure having a first thickness and a second thickness, wherein the first thickness is different from the second thickness.

[006] Additional features and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The features and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[007] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[008] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention and together with the description, serve to explain the principles of the invention.

[009] Figures 1-4 are cross-sectional views of the fabrication steps consistent with one embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[010] Reference will now be made in detail to the present embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[011] Figures 1-4 are cross-sectional views of the fabrication steps consistent with one embodiment of the present invention. Referring to Figure 1, the method of the present invention starts by defining a wafer substrate 10. Substrate 10 may be any known substrate material, such as silicon. A first nitride layer 12 is grown over substrate 10 in a nitrogen environment. This is a pre-nitridation process. In one embodiment, first nitride layer 12 has a thickness of less than or equal to 11 angstroms, and is grown at a temperature ranging from approximately 700°C to 900°C.

[012] The ultra-thin nitride layer 12 leads to a change in the characteristics, such as surface energy, of the surface of substrate 10, such that the surface of substrate 10 exhibits the characteristics of a nitride layer. The change in the state of the substrate surface enables an accelerated deposition rate and an improved deposition ratio of the subsequent formation of a nitride layer over the nitride-like surface of the substrate, as compared to a bare substrate surface. The differences between the method of the present invention and the conventional method of providing a nitride layer over a bare silicon surface are shown in Table 1.

	present method at 900°C	present method at 900°C	present method at 700°C	bare wafer
First Nitride Layer Thickness	11.3	7.6	7.8	0.5
Nitride Thickness after Deposition	36.1	32.6	28.9	18.1
Deposition Rate	3.81 /min	3.85 /min.	3.24 /min.	2.70 /min.
Deposition Ratio	1.41	1.42	1.21	1

Table 1

[013] The second and third columns of Table 1 show the data relative to the formation of a nitride layer in accordance with one method of the present invention performed at 900°C. The fourth column of Table 1 shows the data relative to the formation of a nitride layer in accordance with one method of the present invention performed at 700°C. The fifth column of Table 1 shows the data relative to the formation of a nitride layer in accordance with a conventional method.

[014] Referring to Table 1, the method of the present invention first provides a first nitride layer having a thickness of 11.3 μ , 7.6 μ , and 7.8 μ , respectively. In contrast, the conventional method provides a native nitride with a thickness of about 0.5 μ . In addition, the method of the present invention provides a thicker nitride layer than the conventional method. The formation of the thicker nitride layer is also partly due to the processing conditions of the present invention. For example with reference to Table 1, after first nitride layer 12 is formed to a thickness of 11.3 μ at 900°C consistent with the method of the present invention, a nitride layer formed over first nitride layer 12 with the bare wafer would have a thickness of 18.1 μ . The total thickness of the two nitride layers is 29.4 μ , which is still less than 36.1 μ , the thickness of the nitride layer formed with the method of the present invention. Finally, the method of the present invention provides a superior deposition rate and ratio.

[015] The method of the present invention continues by providing a layer of photoresist (not shown) over first nitride layer 12. Photoresist is patterned and defined using a conventional photolithographic method. Referring to Fig. 2, region 2 of first nitride layer 12 is covered by the photoresist and region 4 of first nitride layer

12 is uncovered by the photoresist. An etch step follows with the patterned and defined photoresist as a mask. After etching, first nitride layer 12 in region 2 remains, and first nitride layer 12 in region 4 is removed. Photoresist is then removed.

[016] Referring to Figure 3, conventional nitridation steps follow to deposit a second layer of nitride 14 over region 2 of first nitride layer 12 and region 4, exposed surface of substrate 10. Deposition of second nitride layer 14 is performed by using low pressure chemical vapor deposition ("LPCVD") or jet vapor deposition ("JVD").

[017] Referring to Figure 4, after nitridation, a nitride layer 16 with two different thicknesses is formed over regions 2 and 4. Specifically, nitride layer 16 includes a first thickness T2 formed over region 2. Thickness T2 is the result of first nitride layer 12 plus nitride layer 14 deposited over first nitride layer 12 in region 2. As an example shown in Table 1, thickness T2 may have a thickness of 36.1 \AA , 32.6 \AA , or 28.9 \AA . Nitride layer 16 also includes a thickness T3 formed over region 4. Thickness T3 is the result of nitride layer 14 formed over bare silicon substrate. An exemplary thickness for thickness T3 is 18.1 \AA as shown in Table 1. It is desirable that thickness T2 is greater than thickness T3 plus the thickness of first nitride layer 12 formed over substrate 10.

[018] A dual gate nitride structure is thus formed. Conventional semiconductor manufacturing processes may then follow to complete the formation of a memory device and other semiconductor structures.

[019] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

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